REMARKS

I. INTRODUCTION

By this Response, claim 3 has been amended and claims 1-33 are currently pending in the application.

Applicants acknowledge that Examiner has acknowledged Applicants' election with traverse of Embodiment 1 (Fig. 3A-3B, claims 1-4, 6, 11, and 12) in the reply filed on 4/14/2003.

In view of the following Remarks, Applicants respectfully request reconsideration and timely withdrawal of the pending objections and rejections for the reasons discussed below.

II. DRAWINGS

On page 2, numbered paragraph 2 of the Office action, the Examiner objected to Fig. 7A of the drawings because the "bottom left corner of Fig. 7A has not been labeled and it is not clear whether it is part of the drawing." To resolve this objection, Applicants have amended the drawing and provided a replacement drawing sheet in compliance with 37 CFR 1.121(d).

Applicants amended Fig. 7A and Fig. 7B and provided a replacement drawing sheet in compliance with 37 CFR 1.121(d). The replacement drawing sheet including amended Fig. 7A and 7B is attached hereto.

Applicants amended Fig. 7A to include reference numeral 731 referring to the bottom left corner of Fig. 7A, which is a void area in the zigzag shape of the offset 730.

Applicants amended Fig. 7B to include reference numeral 731 at two locations related to the offset 730, which are void areas in the zigzag shape of the offset 730.

Accordingly, Applicants amended paragraph [0063] of the specification to additionally recite: "The bottom left corner of the offset region 730 shown in Fig. 7A refers to a void area 731 relating to the zigzag shape of the offset region 730. As shown in the cross-sectional view of the

thin film transistor of Fig. 7B, the offset region 730 has multiple void areas 731 related to the zigzag shape of the offset region 730."

In light of the foregoing amendments, Applicants respectfully request that the objection of Fig. 7A be removed.

On page 3, numbered paragraph 2 of the Office action, the Examiner objected to Fig. 6 and Fig. 7 because they do not include reference numerals 661, 665, and 321, which are mentioned in the description.

To resolve this objection, Applicants amended the specification to properly recite that the source/drain regions are reference numerals 651 and 655, instead of reference numerals 661 and 665. Applicants also amended the specification to recite that the contacts are reference numerals 641 and 645, instead of reference numerals 651 and 655.

Applicants amended Fig. 7B to correct a clerical mistake to change reference numeral 321 to reference numeral 721, which is mentioned in the description.

In light of the foregoing amendments, Applicants respectfully request that the objection of Fig. 6 and Fig. 7B.

In compliance with 37 CFR 1.121(d), Applicants have attached to this Response a replacement drawing that includes the amended Fig. 7A and Fig. 7B.

II. SPECIFICATION

On page 3, numbered paragraph 3 of the Office action, the examiner objected to claim 3 and cited the following informality: "The recitation 'a thin film resistor ...' should read 'a thin film transistor ...'". To resolve this objection, Applicants have amended the specification to

correct the above-identified clerical mistake. Applicants respectfully request that the objection of claim 3 be removed.

REJECTIONS OF CLAIMS 1 and 2 UNDER 35 U.S.C. §102(b) AS BEING ANTICIPATED BY OHTANI, EP 1033755

In the Office Action, at page 4, numbered paragraph 5, claims 1 and 2 were rejected under 35 U.S.C. §102(b) as being anticipated by Ohtani et al., EP 1033755 (hereinafter, "Ohtani") "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 84 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Ohtani does not disclose all of the elements recited in claims 1 and 2 of the present application; therefore, Applicants respectfully traverse this rejection for at least the following reasons.

Claim 1 of the present application recites: "A flat panel display ... wherein a thin film transistor in the pixel array portion has a different resistance value than a thin film transistor in the driving circuit portion."

Ohtani does not teach or suggest there being a thin film transistor in the pixel array portion having a different resistance value than a thin film transistor in the driving circuit portion, as disclosed in claim 1 of the present application. Instead, Ohtani discloses there being a difference in the doping concentration of the LDD region of the thin film transistor (TFT) between the pixel area and the driver region. Therefore, Ohtani specifically describes that the difference in resistance between the LDD region in the pixel region and the LDD region in the driver circuit region is due to differences in the doping concentration. Ohtani does not disclose the resistance of the overall resistance of the TFT. In particular, Ohtani does not disclose the resistance of the gate region, i.e., the channel region. Although the LDD region is described in

Ohtani as being included in the channel region, the gate region (channel region) of the present application is different than the LDD region of Ohtani.

Accordingly, claim 1 of the present application patentably distinguishes over Ohtani because Ohtani fails to disclose the resistance of the channel region or the resistance of the thin film transistor. Therefore, for at least the reasons discussed above, it is respectfully requested that independent claim 1 be allowed.

Claim 2 depends from independent claim 1 and is patentable for at least the reasons discussed above. Accordingly, it is respectfully requested that claim 2 be allowed.

REJECTIONS OF CLAIMS 1 and 2 UNDER 35 U.S.C. §102(b) AS BEING ANTICIPATED BY YAMAZAKI, USPN 5,858,823

In the Office Action, at page 4, numbered paragraph 6, claims 1 and 2 were rejected under 35 U.S.C. §102(b) as being anticipated by Yamazaki et al., EP 1033755 (hereinafter, "Yamazaki"). Yamazaki does not disclose all of the elements recited in claims 1 and 2 of the present application; therefore, Applicants respectfully traverse this rejection for at least the following reasons.

Claim 1 of the present application recites: "A flat panel display ... wherein a thin film transistor in the pixel array portion has a different resistance value than a thin film transistor in the driving circuit portion."

Yamazaki does not teach or suggest there being a thin film transistor in the pixel array portion having a different resistance value than a thin film transistor in the driving circuit portion, as disclosed in claim 1 of the present application. Instead, Yamazaki is directed to a method for crystallizing amorphous silicon, and more particularly, to a technique of

crystallization using nickel as a catalyst. Yamazaki does not disclose that the resistance of the TFT in the pixel area is different than that of the TFT in the driver circuit area.

Accordingly, claim 1 of the present application patentably distinguishes over Yamazaki because Yamazaki fails to disclose that the resistance of the TFT in the pixel area is different than that of the TFT in the driver circuit area. Therefore, for at least the reasons discussed above, it is respectfully requested that independent claim 1 be allowed.

Claim 2 depends from independent claim 1 and is patentable for at least the reasons discussed above. Accordingly, it is respectfully requested that claim 2 be allowed.

REJECTIONS OF CLAIMS 1 and 2 UNDER 35 U.S.C. §102(e) AS BEING ANTICIPATED BY LIN, USPN 5,858,823

In the Office Action, at page 4, numbered paragraph 7, claims 1 and 2 were rejected under 35 U.S.C. §102(e) as being anticipated by Lin et al., US 2004/0096999 (hereinafter, "Lin"). Lin does not disclose all of the elements recited in claims 1 and 2 of the present application; therefore, Applicants respectfully traverse this rejection for at least the following reasons.

Claim 1 of the present application recites: "A flat panel display ... wherein a thin film transistor in the pixel array portion has a different resistance value than a thin film transistor in the driving circuit portion."

Lin does not teach or suggest there being a thin film transistor in the pixel array portion having a different resistance value than a thin film transistor in the driving circuit portion, as disclosed in claim 1 of the present application. Instead, Lin is directed to forming an LDD region for TFTs in a pixel area and a peripheral region. Lin, page 2, paragraphs 18-20. Lin does

not disclose there being any difference in resistance between the TFT of the driver circuit area and that of the TFT in the pixel area.

Accordingly, claim 1 of the present application patentably distinguishes over Lin because Lin fails to disclose that the resistance of the TFT in the pixel area is different than that of the TFT in the driver circuit area. Therefore, for at least the reasons discussed above, it is respectfully requested that independent claim 1 be allowed.

Claim 2 depends from independent claim 1 and is patentable for at least the reasons discussed above. Accordingly, it is respectfully requested that claim 2 be allowed.

REJECTIONS OF CLAIMS 3, 4 and 6 UNDER 35 U.S.C. §102(b) AS BEING ANTICIPATED BY OHTANI, EP 1033755

In the Office Action, at page 5 numbered paragraph 8, claims 3, 4, and 6 were rejected under 35 U.S.C. §102(b) as being anticipated by Ohtani et al., EP 1033755 (hereinafter, "Ohtani"). Ohtani does not disclose all of the elements recited in claims 3, 4, and 6 of the present application; therefore, Applicants respectfully traverse this rejection for at least the following reasons.

Claim 3 of the present application recites: "A flat panel display ...wherein a thin film transistor in the pixel array portion has a different resistance value in its gate region than a thin film transistor in the driving circuit portion."

Ohtani does not teach or suggest there being a thin film transistor in the pixel array portion having a different resistance value in its gate region than a thin film transistor in the driving circuit portion, as disclosed in claim 3 of the present application. As discussed above, Ohtani fails to disclose the resistance of the channel region or the resistance of the thin film

transistor. Therefore, for at least this reason, it is respectfully requested that independent claim 3 be allowed.

Claims 4 and 6 depend from independent claim 3 and are patentable for at least the reasons discussed above. Accordingly, it is respectfully requested that claims 4 and 6 be allowed.

REJECTIONS OF CLAIMS 3, 4 and 6 UNDER 35 U.S.C. §102(e) AS BEING ANTICIPATED BY LIN, USPN 5,858,823

In the Office Action, at page 6, numbered paragraph 9 claims 3, 4 and 6 were rejected under 35 U.S.C. §102(e) as being anticipated by Lin et al., US 2004/0096999 (hereinafter, "Lin"). Lin does not disclose all of the elements recited in claims 3, 4 and 6 of the present application; therefore, Applicants respectfully traverse this rejection for at least the following reasons.

Claim 3 of the present application recites: "A flat panel display ...wherein a thin film transistor in the pixel array portion has a different resistance value in its gate region than a thin film transistor in the driving circuit portion."

Lin does not teach or suggest there being a thin film transistor in the pixel array portion having a different resistance value in its gate region than a thin film transistor in the driving circuit portion, as disclosed in claim 3 of the present application. As discussed above, Lin is directed to forming an LDD region for TFTs in a pixel area and a peripheral region and does not disclose there being any difference in resistance between the TFT of the driver circuit area and that of the TFT in the pixel area. Therefore, for at least this reason, it is respectfully requested that independent claim 3 be allowed.

Accordingly, claim 3 of the present application patentably distinguishes over Lin because Lin fails to disclose that a thin film transistor in the pixel array portion has a different resistance value in its gate region than a thin film transistor in the driving circuit portion. Therefore, for at least this reason, it is respectfully requested that independent claim 3 be allowed.

Claims 4 and 6 depend from independent claim 3 and are patentable for at least the reasons discussed above. Accordingly, it is respectfully requested that claims 4 and 6 be allowed.

REJECTIONS OF CLAIMS 11 and 12 UNDER 35 U.S.C. §102(b) AS BEING ANTICIPATED BY OHTANI, EP 1033755

In the Office Action, at page 6 numbered paragraph 10, claims 3, 4, and 6 were rejected under 35 U.S.C. §102(b) as being anticipated by Ohtani et al., EP 1033755 (hereinafter, "Ohtani"). Ohtani does not disclose all of the elements recited in claims 11 and 12 of the present application; therefore, Applicants respectfully traverse this rejection for at least the following reasons.

Claim 11 of the present application recites: "A flat panel display ...wherein at least one thin film transistor of a plurality of thin film transistors in the pixel array portion has a different resistance value from at least one thin film transistor of a plurality of thin film transistors in the gate driving circuit portion and the data driving circuit portion."

Ohtani does not teach or suggest there being at least one thin film transistor of a plurality of thin film transistors in the pixel array portion has a different resistance value from at least one thin film transistor of a plurality of thin film transistors in the gate driving circuit portion and the data driving circuit portion, as disclosed in claim 11 of the present application. As discussed above, Ohtani fails to disclose the resistance of the channel region or the resistance of the thin

film transistor. Therefore, for at least this reason, it is respectfully requested that independent claim 11 be allowed.

Claim 12 depends from independent claim 11 and is patentable for at least the reasons discussed above. Accordingly, it is respectfully requested that claim 12 be allowed.

REJECTIONS OF CLAIMS 3, 4 and 6 UNDER 35 U.S.C. §102(e) AS BEING ANTICIPATED BY LIN, USPN 5,858,823

In the Office Action, at page 7, numbered paragraph 11, claims 11 and 12 were rejected under 35 U.S.C. §102(e) as being anticipated by Lin et al., US 2004/0096999 (hereinafter, "Lin"). Lin does not disclose all of the elements recited in claims 11 and 12 of the present application; therefore, Applicants respectfully traverse this rejection for at least the following reasons.

Claim 11 of the present application recites: "A flat panel display ...wherein at least one thin film transistor of a plurality of thin film transistors in the pixel array portion has a different resistance value from at least one thin film transistor of a plurality of thin film transistors in the gate driving circuit portion and the data driving circuit portion."

Lin does not teach or suggest there being at least one thin film transistor of a plurality of thin film transistors in the pixel array portion has a different resistance value from at least one thin film transistor of a plurality of thin film transistors in the gate driving circuit portion and the data driving circuit portion, as disclosed in claim 11 of the present application. As discussed above, Lin is directed to forming an LDD region for TFTs in a pixel area and a peripheral region and does not disclose there being any difference in resistance between the TFT of the driver circuit area and that of the TFT in the pixel area. Therefore, for at least this reason, it is respectfully requested that independent claim 11 be allowed.

Claim 12 depends from independent claim 11 and is patentable for at least the reasons discussed above. Accordingly, it is respectfully requested that claim 12 be allowed.

IV. CONCLUSION

It is respectfully requested that this amendment be entered prior to the examination of the above-referenced patent application. Applicants respectfully submit that the claims as presented are patentable over the prior art of record, request reconsideration and withdrawal of the objections and rejections to the claims, and request that the claims be passed to issuance. If the Examiner desires any additional information, the Examiner is invited to contact applicants' attorney at the telephone number listed below to expedite prosecution.

Respectfully submitted,

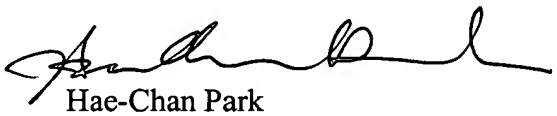

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FIG. 7A

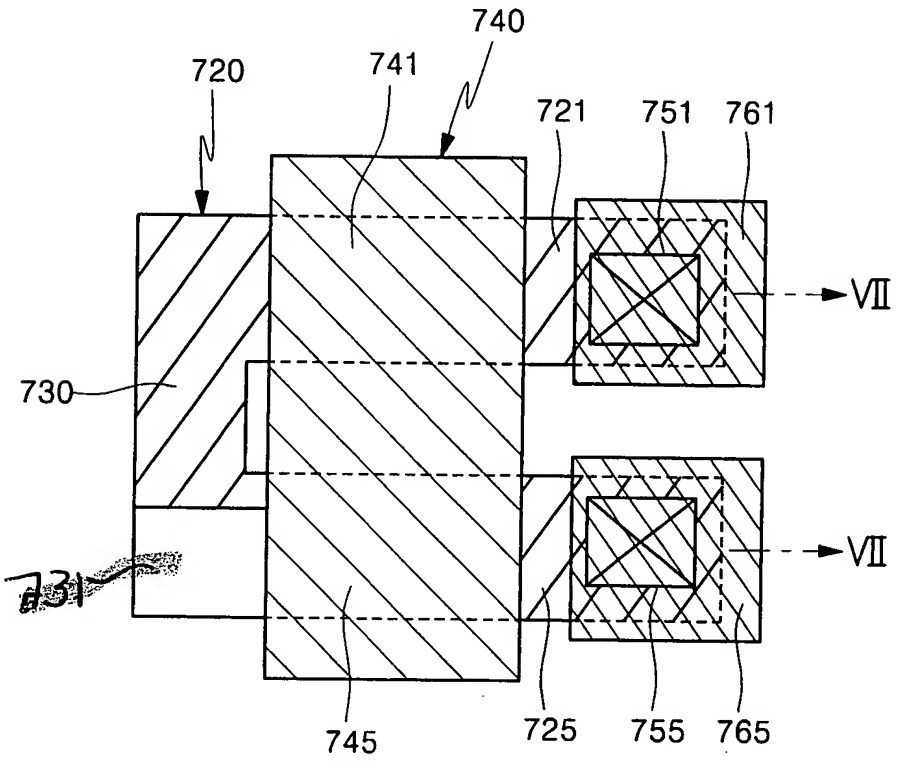

FIG. 7B